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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,898	01/09/2002	Jong-Hong Bae	P67539US0	8890

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,898	BAE, JONG-HONG	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because of the use of legal phraseology such as "means" and a minor informality on line 11 with the sentence containing "output pin is in a system mode". Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because it is replete with informalities, examples of which are the following: "there is provide" on line 6 of page 3 should be "there is provided"; "output pin is in a system mode" on line 14 of page 3 should be "output pin in a system mode"; "there is provide" on line 19 of page 3 should be "there is provided"; "clock generator 200 is included" on line 7 of page 5 should be "clock generator 100 is included"; "clock" on line 3 of page 6 is misspelled; "the MDS system is below to the maximum operating frequency" on line 19 of page 7 should be "the MDS system is below the maximum operating frequency"; and etc. The disclosure should be revised carefully, with no new subject matter, to remove all informalities. Appropriate correction is required.

4. Claims 1 and 7 are objected to because of the following informalities: "...for using the clock output pin is in a system mode" is grammatically incorrect; "a microcontroller" on lines 10-11 and 19-20, respectively, should be "the microcontroller" as it is referring to the antecedent established in the preamble. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams, US Patent 6745338, in view of Hui et al., US Patent 6694463, hereinafter Hui.

7. Williams discloses a microcontroller [circuit 100], comprising [fig.2; col.2, ll.43-51]:

- A clock input pin [102], wherein an input signal [clk_in] from the external circuit [106] is inputted.
- A clock generating means [120] for generating a clock signal [126] by receiving a signal from the clock input pin.
- A clock output pin [104] for receiving an output signal [clk_out] of the clock generating means and outputting the output signal.

8. Williams did not disclose the details of transmitting an internal signal.

9. Hui discloses a microcontroller [integrated circuit device] comprising [fig.2; col.3, ll.19-61]:

- A first switch [test_en 41 of test mode input buffer 44] for transmitting an internal signal [27 from other internal logic 39] of the microcontroller to the output pin [32] for using the clock output pin in a system mode [normal operating mode].
- A second switch [test_en 41 of test mode output buffer 46], which is enabled [first state] when the generating means [circuit operates under some generating means in the broadest interpretation for testing] is operated in the generation mode [test operating mode] and disabled [second state] when the microcontroller is operated in the system mode [normal operating mode].

10. It would have been obvious to one of ordinary skill in the art, having the teachings of Williams and Hui before him at the time the invention was made, to modify the microcontroller taught by Willaims to include the switches taught by Hui, in order to obtain the microcontroller comprising a first switch for transmitting an internal signal of a microcontroller to the clock output pin for using the clock output pin is in a system mode and a second switch, which is enabled when the clock generating means is operated in the clock generation mode and disabled when the microcontroller is operated in the system mode. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to test for continuity in a circuit device [Hui: col.1, ll.13-58].

11. As to claim 2, Hui discloses, wherein a second switch [227] includes a plurality of switches connected in parallel [fig.5; col.3, l.62 – col.4, l.14; multiple switches in mux to select appropriate path].

12. As to claim 3, Williams discloses, comprising a control means [122' generating clk-mode] for controlling of switches [to 130' and 132'] depending on a clock signal [clk_in] of the

clock input pin [102] [fig.5; col.4, l.61 – col.5, l.34] and Hui discloses, comprising a control means [41 generated by chip] for selectively controlling each of switches [fig.5; mux 28..228 and 227 selectively controlled by test_eni].

13. As to claim 4, Hui discloses, comprising a control means [41 generated by chip] for selectively enabling first and second switches classified by modes [states] [col.3, ll.19-39].

14. As to claim 5, Williams and Hui disclose each and every limitation as set forth above in reference to claims 3 and 4.

15. As to claim 6, Williams discloses, wherein the clock generating means [120] includes [fig.3; col.2, l.65 – col.3, l.13]:

- An inverter [130] for amplifying an input signal [clk_in, 124] as a full-swing to generate a clock signal [clk_out, 126].
- A resistor [rfb 132], which is connected to input and output terminals of the inverter [fig.3].

16. In re claim 7, Williams and Hui disclose every limitation as set forth above in reference to claim 1. In particular Williams discloses a system [fig.2] having a microcontroller [circuit 100], comprising:

- A first clock generating means [120] for receiving a signal [124] from the clock input pin to generate a clock signal [126] [fig.2; col.2, ll.43-51].
- A second clock generating means [external based clock] for providing a clock signal to the microcontroller through the clock input pin in a system mode [clock mode at first state] [col.3, ll.47-65].

17. As to claim 8, Williams and Hui disclose each and every limitation as set forth above in reference to claims 2 and 7.

18. As to claim 9, Williams discloses, comprising a control means [122' generating clk-mode], which is placed in the inside of the microcontroller [fig.5], for controlling of switches [to 130' and 132'] depending on a frequency of a clock signal [clk_in] of the clock input pin [102] [fig.5; col.3, ll.47-57; col.4, l.61 – col.5, l.34] and Hui discloses, comprising a control means [41 generated by chip] for selectively controlling each of switches [fig.5; mux 28..228 and 227 selectively controlled by test_eni].

19. As to claim 10, Williams and Hui disclose each and every limitation as set forth above in reference to claims 4 and 9.

20. As to claim 11, Williams and Hui disclose each and every limitation as set forth above in reference to claims 9 and 10.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited U.S. patent documents describe various methods and systems associated with clock sources and output ports.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
December 14, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER ~~3600~~ 2100